

ABSTRACT OF THE DISCLOSURE

Methods and devices are disclosed utilizing a polysilicon wings or ears in a stacked gate region. The stacked gate region includes a substrate, at least one trench, an oxide layer, at 5 least one floating gate layer and at least one polysilicon wing. The substrate has at least one semiconductor layer. The at least one trench is formed in the substrate and filled with an oxide. The oxide layer is formed over the substrate and the trench. The at least one floating gate layer is formed over the oxide layer. The at least one polysilicon wing is formed adjacent to vertical edges of the at least one floating gate layer and over the oxide layer. The present invention includes polysilicon wings or ears which can increase the capacitive coupling of memory cells in memory devices in which they are used. Generally, the polysilicon wings or ears are placed proximate to the floating gate of a memory cell. Thus, the present invention may allow for further reducing or scaling the size of memory cells and devices.

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